Computer Architecture

1. [20%] A program runs in 10 seconds o computer A, which has a 2 GHz clock. We are trying to help a computer designer build a computer, B, which will run this program in 6 seconds. The designer has determined that a substantial increase in the clock rate is possible, but this increase will affect the rest of the CPU design, causing computer B to require 1.2 times as many clock cycles as computer A for this program. What clock rate should we tell the designer to target?

2. [20%] There are four steps in transforming a C program in a file on disk into a program running on a computer. Please give the four steps and describe them briefly.

3. [10%] Show the IEEE 754 binary representation of the number -0.75_{ten} in single precision.

4. [15%] Please explain what is **translation-lookaside buffer** (TLB)? Please also explain what is the difference between **TLB miss** and **page fault**.

5. [15%] Please explain what is **polling**, **interrupt-driven**, and **DMA** for interfacing I/O device.

6. [20%] In the following MIPS code sequence, please identify the places of **pipeline data hazard**. Please also explain how to solve them using **forwarding**.

```
sub $2,  $1, $3
and $12, $2, $5
or  $13, $6, $2
add $14, $2, $2
sw  $15, 100($2)
```