Computer Architecture PhD Qualifying Exam

1. [11 points] Pipelining is used to improve the performance of processors. An ideal pipelined processor achieves CPI (clocks per instruction) = 1. However, such ideal case is impossible to achieve due to many factors. What are these factors? Give an example for each factor.

2. [12 points] Superscalar and VLIW can possibly issue or complete at least two instructions in each clock cycle. What are their differences? Give their pros and cons.

3. [12 points] Consider a virtual memory system with the following properties: 38-bit virtual byte address, 16-KB pages, and 32-bit physical byte address. What is the total size of the page table for each process on this machine, assuming that the valid, protection, dirty, and use bits take a total of 4 bits and that all the virtual pages are in use? (Assume that disk addresses are not stored in the page table.)

4. [20 points] Suppose there is a machine called single instruction computer which has only one instruction: Subtract and Branch if Negative (*sbn*). The *sbn* instruction has three operands, each consisting of the address of a word in memory:

    sbn a, b, c

    The instruction will subtract the number in memory location *b* from the number in location *a* and place the result back in *a*, overwriting the previous value. If the result is greater than or equal to 0, the computer will take its next instruction from the memory location just after the current instruction. Please write a program for this machine to add *a* and *b*, leaving the result in *a* and leaving *b* unmodified.

5. [15 points] You are going to enhance a machine, and there are two possible improvements: either make multiply instructions run four times faster than before, or make memory access instructions run two times faster than before. You repeatedly run a program that takes 100 seconds to execute. Of this time, 20% is used for multiplication, 50% for memory access instructions, and 30% for other tasks. What will the speedup be if you improve only multiplication? What will the speedup be if you improve only memory access? What will the speed up be if both improvements are made?

6. [15 points] Consider a three-level memory hierarchy of the form (M_1, M_2, M_3)

where M_1 is connected directly to the CPU. Let c_i and S_i denote the cost per bit and total storage capacity of M_i for i=1,2,3. Let t_{Ai} be the access time of M_i, i.e., the average time to read one word from M_i to its own output port. Let H_i be the hit ratio of M_i. Determine the average cost per bit c and the average access time t_A (with respect to the CPU).

Note: In an n-level memory, the hit ratio H_i associated with the memory M_i at level I may be defined as the probability that the information requested by the CPU has been assigned to M_i.

7. [15 points] A conventional microprogrammed CPU is being redesigned for implementation as a one-chip microprocessor. At present it has a single 256×80-bit control memory, and employs a highly parallel horizontal microinstruction format in which every instruction contains one 8-bit branch address. It is estimated that in a two-level organization of the control unit, only about 64 300-bit nanoinstructions would be needed to implement the current instruction set. If the total size of the control memories is the major cost consideration, should the new microprocessor have one or two-level control? Show your calculations and state all your assumptions.