1. (18%) There are situations in pipelining when the next instruction cannot execute in the following clock cycle. These events are called hazards. Please explain the three types of hazards in detail.

2. (10%) Associativity usually improves the miss ratio, but not always. Give a short series of address references for which a two-way set-associative cache with LRU replacement would experience more misses than a direct-mapped cache of the same size.

3.
   a. (6%) Assume that in a computer the single precision representation of floating point numbers uses 32 bits, in which 8 bits are used for the exponent and 1 bit for the sign. Also assume that the double precision representation uses 64 bits, in which 11 bits are used for the exponent and 1 bit for the sign. Find the binary representation of the number -0.75_{ten} in single and double precision.
   b. (8%) Assume that a second computer has the same lengths for the single precision representation and the double precision representation. However, the second computer uses the IEEE 754 standard, in which floating point numbers are expressed as $(-1)^s \times (1 + significand) \times 2^{(exponent-bias)}$. Find the IEEE 754 binary representation of the number -0.75_{ten}. Assume that bias is 127 for both representations.
   c. (8%) Explain why the IEEE 754 uses a bias in the floating point representation.

4. (15%) Consider a machine with a 2 ns clock, a miss penalty of 20 clock cycles, a miss rate of 0.05 misses per reference. Assume 1.5 references per instruction and a CPI without cache misses of 1. Please calculate the performance in million instructions per second for this machine.

5. (10%) Please briefly explain RISC and CISC, please also provide examples of RISC/CISC, and compare the advantages and disadvantages between them.

6. (10%) Please briefly explain the following terms: (a) Microprogramming (b) Booth's Algorithm

7. (15%) Assume that there are three machines. The first machine (M1) with a 850 MHz clock uses the multicycle datapath in our text book. The second machine (M2) with 700 MHz clock is like M1, except that register updates are done in the same clock cycle as a memory read or ALU operation. Thus, states 6 and 7 can be combined, as well as states 3 and 4. The third machine (M3) with 650 MHz clock is like M2, except that effective address calculations are done in the same clock cycle as a memory access. Thus, states 2, 3, and 4 can be combined, as can 2 and 5, as well as 6 and 7. Suppose the instruction mix is {Loads 20%, Stores 30%, R-type 30%, Branch 10%, and Jump 10%}, find out which machine is fastest and which machine is slowest. (20 pts)