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Part I: Operating System

1. **(7%)** When the physical memory of a computer system is large enough such that the total size of the virtual memory (over all programs) is guaranteed to be smaller than the physical memory, do we still need virtual memory address translation? Explain your answer.
2. **(7%)** What is the FIFO with second chance page replacement policy? How does it compare to the plain FIFO policy?
3. **(8%)** What is a microkernel? What is the role of a microkernel in a computer system? How does it compare to a monolithic kernel?
4. **(8%)** What are the two major approaches to implement a thread package? What are their relative advantages and disadvantages?
5. **(10%)** Describe the necessary conditions for a deadlock to occur. We can prevent deadlock by attacking any one of the conditions. For each condition above, briefly describe the general approach of deadlock prevention by attacking that condition.
6. **(10%)**
   (a) Please explain the terminology: Spin Lock. (2%)
   (b) Please describe the difference between "counting semaphore" and "binary semaphore"? (4%)
   (c) The reader-writer problem is one of the classical synchronization problems. In the solution of the readers-writers problem, the reader process shares the following data structures:

```
semaphore mutex, wrt ;
int readcount;
```

   The semaphores mutex and wrt are initialized to 1; readcount is initialized to 0. The structures of the writer process and the reader process are as underlying statements. Are there any problems with the structures of the writer and the reader processes? If yes, please explain why and give the correct solution. If no, please give the reasons to prove that the structure is correct? (4%)

- The structure of the writer process

```
wait (wrt);
.....
writing is performed
.....
```

- The structure of the reader process

```
readcount++;
```

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```
if (readcount ==1)
    wait(wrt);
  …..
Reading is performed
  …..
readcount--;
if (readcount ==0)
   signal(wrt);
```

Part II: Computer Organization

7. **(10%)** Assume that a processor is a load-store RISC CPU, running with 600MHz. The instruction mix and clock cycles of a program as follows:

Instruction type	Frequency	Clock cycles
A	25%	2
B	10%	2
C	15%	3
D	30%	4
E	20%	1

   (a) Find the CPI. (5%)

   (b) Find the MIPS. (5%)

8. **(10%)** We make an enhancement to a computer that improves some mode of execution by a factor of 10. Enhanced mode is used 80% of the time, measured as a percentage of the execution time when the enhanced mode is in use.

   (a) What is the speedup we have obtained from fast mode? (5%)

   (b) What percentage of the original execution time has been converted to fast mode? (5%)

   Hint: The Amdahl's Law depends on the fraction of the original, unenhanced execution time that could make use of enhanced mode. Thus, we cannot directly use this 80% measurement to compute speedup with Amdahl's Law.

9. **(10%)** The following code fragment processes two arrays and produces an important value in register $v0. Assume that each array consists of 1000 words indexed 0 through 999, that the base addresses of the arrays are stored in $a0 and $a1 respectively, and their size (1000) are stored in $a2 and $a3, respectively. Assume the code is run on a machine with 1 GHz clock. The required number of cycles for instructions **add**, **addi** and **sll** are all 1 and for instructions **lw** and **bne** are 2. In the worst case, how many seconds will it take to execute this code?

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```
        sll     $a2, $a2, 2
        sll     $a3, $a3, 2
        add     $v0, $zero, $zero
        add     $t0, $zero, $zero
outer:  add     $t4, $a0, $t0
        lw      $t4, 0($t4)
        add     $t1, $zero, $zero
inner : add     $t3, $a1, $t1
        lw      $t3, 0($t3)
        bne     $t3, $t4, skip
        addi    $v0, $v0, 1
skip :  addi    $t1, $t1, 4
        bne     $t1, $a3, inner
        addi    $t0, $t0, 4
        bne     $t0, $a2, outer
```

10. **(5%)** Draw the gates for the Sum bit of an adder for the following equation ($\bar{a}$ means NOT a).

$$\text{Sum} = (a \cdot \bar{b} \cdot \overline{\text{CarryIn}}) + (\bar{a} \cdot b \cdot \overline{\text{CarryIn}}) + (\bar{a} \cdot \bar{b} \cdot \text{CarryIn}) + (a \cdot b \cdot \text{CarryIn})$$

11. (10%)

(a) Please explain the difference between "write-through" policy and "write-back" policy? (5%)

(b) Assume that the instruction cache miss rate is 4% and the data cache miss rate is 5%. If a processor has a CPI of 2.0 without any memory stalls and the miss penalty is 200 cycles for all misses, determine how much faster a processor would run with a perfect cache that never missed? Here, the frequency of loads and stores is 35%. (5%)

12. **(5%)** Please explain the following terms: (a) compulsory misses, (b) capacity misses, and (c) conflict misses.