Computer Architecture & Organization

1. [15%] Consider the following performance measurements for a program. Which computer has the higher MIPS rating? Which computer is faster? What is the speedup?

Measurement	**Computer A**	**Computer B**
Instruction Count	10billion	8billion
Clock rate	4GHz	4GHz
CPI	1.0	1.1

2. [15%] Please write a MIPS program that is equivalent to ***if $1<=$2 $1=$1+$2***

3. [10%] What is the difference of **instruction-level parallelism** and **data-level parallelism**? Please provide examples.

4. [10%] What is the difference of **overflow** and **underflow**? Please provide examples.

5. [20%] The division of an instruction into five stages means a five-stage pipeline, which in turn means that up to five instructions will be in execution during any single clock cycle. Thus we separate the datapath into five pieces, with each piece named corresponding to a stage of instruction execution. Please describe the five stages briefly.

6. [20%] Assume an instruction cache miss rate for gcc of 2% and a data cache miss rate of 4%. If a machine has a CPI of 2 without any memory stalls and the miss penalty is 40 cycles for all misses, determine how much faster a machine would run with a perfect cache that never missed. Use the instruction frequencies for gcc in the following table.

Core MIPS	Name	gcc	spice	Arithmetic core + MIPS I	Name	gcc	spice
add	add	0%	0%	FP add double	add.d	0%	4%
add immediate	addi	0%	0%	FP subtract double	sub.d	0%	3%
add unsigned	addu	9%	10%	FP multiply double	mul.d	0%	5%
add immediate unsigned	addiu	17%	1%	FP divide double	div.d	0%	2%
subtract unsigned	subu	0%	1%	load word to FP single	l.s	0%	24%
and	and	1%	0%	store word to FP single	s.s	0%	9%
and immediate	andi	2%	1%	branch on FP true	bclt	0%	1%
shift left logical	sll	5%	5%	branch on FP false	bclf	0%	1%
shift right logical	srl	0%	1%	FP compare double	c.x.d	0%	1%
load upper immediate	lui	2%	6%	move to FP	mtc1	0%	2%
load word	lw	21%	7%	move from FP	mfc2	0%	2%
store word	sw	12%	2%	convert float integer	cut	0%	1%
load byte	lb	1%	0%	shift right arithmetic	sra	2%	0%
store byte	sb	1%	0%	load half	lh	1%	0%
branch on equal (zero)	beq	9%	3%	branch less than zero	bltz	1%	0%
branch on not equal (zero)	bne	8%	2%	branch greater or equal zero	bgez	1%	0%
jump and link	jal	1%	1%	branch less or equal zero	blez	0%	1%
jump register	jr	1%	1%				
set less than	slt	2%	0%				
set less than immediate	slti	1%	0%				
set less than unsigned	sltu	1%	0%				
set less than imm. uns.	sltiu	1%	0%				

FIGURE 4.54 The frequency of the MIPS instructions for two programs, gcc and spice. Calculated from "pixie" output of the full MIPS I. (Pixie is an instruction measurement tool from MIPS.) All instructions that accounted for at least 0.5% of the instructions executed in either gcc or spice are included in the table. Thus the integer multiply and divide instructions are not listed because they were responsible for less than 0.5% of the instructions executed. Pseudoinstructions are converted into MIPS I before execution, and hence do not appear here.

7. [10%] The substantial differences between the circumstances under which a processor-memory bus and an I/O bus or backplane bus are designed lead to two different schemes for communication on the bus: synchronous and asynchronous. Please explain the two terms.