

Computer Organization Ph.D. Candidate Exam.

1. [10%] Suppose we have two implementations of the same instruction set architecture. Machine A has a clock cycle time of 1ns and a CPI of 2.0 for some program, and machine B has a clock cycle time of 2 ns and CPI of 1.2 for the same program. Which machine is faster for this program, and by how much?

2. [20%] One simple way to model time for logic is to assume each AND or OR gate takes the same time for a signal to pass through it. Time is estimated by simply counting the number of gates along the longest path through a piece of logic. Compare the number of gate delays for the critical paths of two 16-bit adders, one using ripple carry and one using two-level carry lookahead.

3. [20%] The arithmetic-logical (or R-type) instruction datapath of Fig.1 and the memory instruction datapath of Fig.2 are quite similar. The key differences are the following:

- The second input to the ALU unit is either a register (if it's an R-type instruction) or the sign-extended lower half of the instruction (if it's a memory instruction).
- The value stored into a destination register comes from the ALU (for an R-type instruction) or the memory (for a load).

Show how to combine the two datapaths using multiplexors, without duplicating the functional units that are in common in Fig.1 and Fig.2. Ignore the control of the multiplexors.

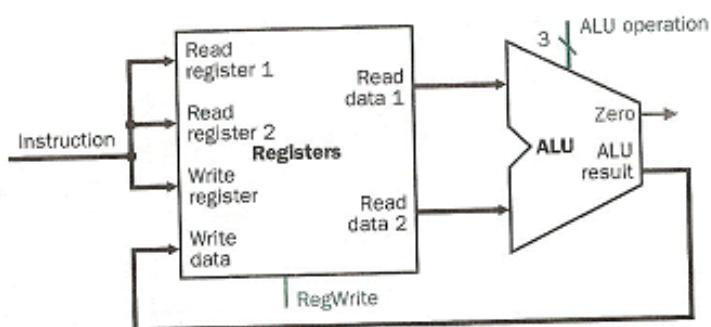


Fig.1 The datapath of R-type instructions

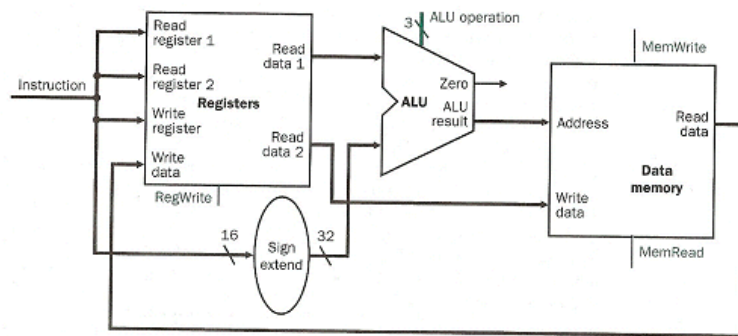


Fig.2 The datapath for a load or store does a register access, followed by a memory address calculation, then a read for write from memory, and a write into the register file if the instruction is a load.

4. [15%] Consider a loop branch that branches nine times in a row, then is not taken once. Assuming a one-bit dynamic branch prediction scheme is used and the prediction bit for this branch remains in the prediction buffer, what is the prediction accuracy for this branch? Please justify your answer.

5. [15%] Assuming a machine uses 32-bit address and a direct-mapped cache with 16KB of data and 4-word blocks, how many total bits are required for the cache? (hint: in addition to the tag and data, a valid bit is required for each entry in the cache)

6. [20%] Please explain the following terms: (a) Translation-lookaside buffer (b) Direct memory access (c) Pipeline data hazard (d) Exception program counter