Computer Organization (Ph.D. Candidacy)

1. (20%) Consider the machine with three instruction classes and CPI measurements as follows:

Instruction class	CPI for this instruction class
A	1
B	2
C	3

Now suppose we measure the code for the same program from two different compilers and obtain the following data:

Code from	Instruction counts (in billions) for each instruction class		
	A	B	C
Compiler A	5	1	1
Compiler B	10	1	1

Assume that the machine's clock rate is 500 MHz. Which code sequence will execute faster according to MIPS? According to execution time?

2. (10%) The representation of a MIPS floating-point number is shown as (*s*, *exponent*, *significand*), where *s* is the sign of the floating-point number (1 means negative), *exponent* is the value of the 8-bit exponent field (including the sign of the exponent), and *significand* is the 23-bit number in the fraction. What decimal number is represented by this word?

1	1	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

3. (20%) A program runs in 10 seconds on computer A, which has a 400-MHz clock. We are trying to help a computer designer build a machine, B, that will run this program in 6 seconds. The designer has determined that a substantial increase in the clock rate is possible, but this increase will affect the rest of the CPU design, causing machine B to require 1.2 times as many clock cycles as machine A for this program. What clock rate should we tell the designer to target?
4. (20%) Using MIPS assembly language, please provide an example code sequence with **Data Hazard** and explain how the problem can be solved using **Forwarding**. The example sequence should be short and contain no more than three instructions.
5. (15%) Assume an instruction cache miss rate for a program is 2% and a data cache miss rate is 4%. Suppose the frequency of all memory access instructions (load and store) is 50%. If a processor has a CPI of 3 without any memory stalls and the miss penalty is 50 cycles for all misses, determine how much faster a processor would run with a perfect cache that never missed.
6. (15%) Assuming that we have an array of four independent disks in that data are spreading over disks (RAID 0). Suppose each disk has 16 sectors per track, each sector holds 1KB of data, and the disk revolves at 3750 RPM. Assume that the average seek time is 2 ms, the delay of the disk controller is 1 ms per transaction, and the requests are random reads of 4 KB of data from sequential sectors. Please calculate the performance in KB per second for this disk system.