Computer Architecture & Organization

1. (20%) Increasing associativity requires more comparators, as well as more tag bits per cache block. Assuming a cache of 4K blocks, a four-word block size, and a 32-bit address, find the total number of sets and the total number of tag bits for caches that are direct mapped, two-way and four-way set associative, and fully associative.

2. (15%) In a computer, system the various subsystems must have interfaces to one another. This is commonly done with a bus, which is a shared communication link. A bus generally contains a set of control lines and a set of data lines. Buses are traditionally classified as one of three types: processor-memory buses, I/O buses, and backplane buses. Please explain the three types of buses.

3. (15%) Please explain the following three misses in a memory: (a) compulsory misses, (2) capacity misses, (3) conflict misses.

4. (10%) Find the IEEE 754 binary representation of the number -3.8_{ten} in single precision.

5. (10%) Please briefly explain RISC and CISC, please also provide examples of RISC/CISC, and compare the advantages and disadvantages between them in terms of IC, CPI, and CCT.

6. (10%) Assume that memory access instructions take 4 cycles and account for 40% of execution time. The other instructions require an average of 3 cycles for each instruction. What is the frequency of memory access instructions?

7. (5%) What are pros and cons of single and multiple cycle implementation in the design of datapath?

8. (15%) Please briefly explain the following terms: (a) Microprogramming (b) Amdahl's Law (c) Overflow