國立東華大學資訊工程系博士班資格考
Computer Architecture, Fall 2007

1. [20%] Please briefly explain what is (a) microprogramming (b) multicycle implementation (c) Amdahl's law (d) pseudodirect addressing
2. [15%] Given the following instruction distributions and cycle times for a MIPS machine, how much percentage of time is spent on data memory access instructions?

Instruction Type	Frequency	CPI
ALU ops	40%	4
Loads	20%	4
Stores	10%	5
Branches	30%	3

3. [15%] Show the IEEE 754 binary representation for the decimal floating-point number -7.7 in single precision.
4. [15%] Consider the pipelined control using the instruction mix for gcc. The instruction mix for gcc is 23% loads, 13% stores, 19% branches, 2% jumps, and 43% all the rest of the mix. The operation times for the major functional units are 2 ns for memory access, 2 ns for ALU operation, and 1 ns for register file read or write. For pipelined execution, assume that half of the load instructions are immediately followed by an instruction that uses the result, that the branch delay on misprediction is 1 clock cycle, and that one-quarter of the branches are mispredicted. Assume that jumps aloays pay 1 full clock cycle of delay, so their average time is 2 clock cycles. What's the average instruction time in nanoseconds?
5. [20%] Suppose we have a processor with a based CPI of 1.0, assuming all references hit in the primary cache, and a clock rate of 500 MHz. Assume a main memory access time of 200 ns, including all the miss handling. Suppose the miss rate per instruction at the primary cache is 5%. How much faster will the machine be if we add a seconday cache that has a 20-ns access time for either a hit or a miss and is large enough to reduce the miss rate to main memory to 2%.
6. [15%] Suppose we have a processor which executes with a 500-MHz clock and hard disk with transfer speed of 4MB/sec. Assume that the initial setup of a DMA transfer takes 1000 clock cycles for the processor, and assume the handling of the interrupt at DMA completion requires 500 clock cycles for the processor. The hard disk has a transfer rate of 4MB/sec and uses DMA. If the average transfer from the disk is 8KB, what fraction of the 500-MHz processor is consumed if the disk is actively transferring 100% of the time? Ignore any impact from bus contention between the processor and DMA controler.