Computer Architecture PhD Qualifying Exam

Fall 2005

1. [20%] Our favorite program runs in 10 seconds on computer A, which has a 400-MHz clock. We are trying to help a computer designer build a machine, B, that will run this program in 6 seconds. The designer has determined that a substantial increase in the clock rate is possible, but this increase will affect the rest of the CPU design, causing machine B to require 1.2 times as many clock cycles as machine A for this program. What clock rate should we tell the designer to target?

2. [20%] Suppose we have a processor with a base CPI of 1.0, assuming all references hit in the primary cache, and a clock rate of 500MHz. Assume a main memory access time of 200 ns, including all the miss handling. Suppose the miss rate per instruction at the primary cache is 5%. How much faster will the machine be if we add a secondary cache that has a 20-ns access time for either a hit or a miss and is large enough to reduce the miss rate to main memory to 2%.

3. [10%] It is the compiler's job to associate program variables with registers. Consider the C assignment statement $F = (g+h)-(i+j)$, where the variables *f, g, h, i* and *j* can be assigned to the registers *$s0, $s1, $s2, $s3,* and *$s4,* respectively. What is the compiled MIPS assembly code?

4. Cache:
   (a) [5%] Why do we need a valid bit for each block in the cache?
   (b) [5%] For a fully associative cache or set associative cache, we need a tag for each block. Why?
   (c) [8%] Give two techniques that can reduce cache miss rate. Briefly explain them.

5. [12%] Explain what polling (programmed I/O) and interrupt are. What are their advantages and disadvantages respectively?

6. [20%] Consider a virtual memory system with the following properties: 38-bit virtual byte address, 16-KB pages, and 32-bit physical byte address. What is the total size of the page table for each process on this machine, assuming that the valid, protection, dirty, and use bits take a total of 4 bits and that all the virtual pages are in use? (Assume that disk addresses are not stored in the page table.)