## Computer Organization for Ph.D. Candidacy

1. $(20 \%)$ A program runs in 10 seconds on machine A , which has a $400-\mathrm{MHz}$ clock. Machine B is designed to run the same program in 6 seconds. The designer has determined that a substantial increase in the clock rate is possible, but this increase will affect the rest of the CPU design, causing machine B to require 1.2 times as many clock cycles as machine A for this program. What clock rate should we tell the designer to target?
2. (20\%) Consider the machine with three instruction classes and CPI measurements as follows:

| Instruction class | CPI for this instruction class |
| :---: | :---: |
| A | 1 |
| B | 2 |
| C | 3 |

Now suppose we measure the code for the same program from two different compilers and obtain the following data:

| Code from | Instruction counts (in billions) for each instruction class |  |  |
| :---: | :---: | :---: | :---: |
|  | A | B | C |
| Compiler A | 5 | 1 | 1 |
| Compiler B | 10 | 1 | 1 |

Assume that the machine's clock rate is 500 MHz . Which code sequence will execute faster according to MIPS? According to execution time?
3. (10\%) The representation of a MIPS floating-point number is shown as (s, exponent, significand), where $s$ is the sign of the floating-point number (1 means negative), exponent is the value of the 8 -bit exponent field (including the sign of the exponent), and significand is the 23-bit number in the fraction.

What decimal number is represented by this word?

| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |

4. (20\%) What is the difference of instruction-level parallelism and data-level parallelism. Please provide an example for each one.
5. (15\%) Suppose we have a processor with a base CPI of 1.0, assuming all references hit in the primary cache, and a clock rate of 4 GHz . Assume a main memory access time of 100 ns , including all the miss handling. Suppose the miss rate per instruction at the primary cache is $2 \%$. How much faster will the processor be if we add a secondary cache that has a 12.5 ns access time for either a hit or a miss and is large enough to reduce the miss rate to main memory to $0.5 \%$ ?
6. (15\%) What is the average disk access time to read or write a 512B sector for a disk rotating at 15,000 RPM with average seek time of 0.7 ms , a $10 \mathrm{MB} / \mathrm{sec}$ transfer rate, and a 0.2 ms controller overhead?
